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Iterative Demodulation and Decoding for Parallel Combinatorial SS Systems

Ken-ichi TAKIZAWA[†a)], ***Student Member***, **Shigenobu SASAKI**[††], **Shogo MURAMATSU**[††], ***and*** **Hisakazu KIKUCHI**[††], ***Regular Members***

SUMMARY This paper proposes iterative demodulation/decoding for parallel combinatorial spread spectrum (PC/SS) systems. A PC/SS system conveys information data by a combination of pre-assigned orthogonal spreading sequences with polarity. In this paper, convolutional coding with a uniform random interleaver is implemented in channel coding, just like as a serial concatenated coding. A 'soft-in/soft-out' PC/SS demodulator based on a posteriori probability algorithm is proposed to perform the iterative demodulation and decoding. Simulation results demonstrate that the proposed iterative demodulation/decoding scheme bring significant improvement in bit error rate performance. This proposed decoding scheme achieves high-speed transmission by two approaches. One is a puncturing operation, and the other is to increase the number of transmitting sequences. In the latter approach, lower error rate performance is achieved comparing with that the punctured convolutional code is used to increase the information bit rate.

key words: *spread spectrum, multi-code CDMA, iterative decoding, channel coding*

1. Introduction

Direct sequence spread spectrum (DS/SS) technique has widely spread in various wireless communication applications. It is applied to the code division multiple access (CDMA) air interface in the third generation mobile communications [1], [2] and to an anti-interference technique in wireless LAN systems [3].

We have to consider two points on the DS/SS technique to apply it to future wireless multimedia communication networks. The first point is how to transmit high-speed data under a limited available bandwidth. Possible candidates for high-speed data transmission in DS/CDMA are orthogonal multi-code CDMA [4] and multi-carrier CDMA [5]. We are going to focus on the multi-code CDMA systems in this paper.

As high-speed data transmission technique in multi-code DS/CDMA, we have proposed the parallel combinatorial SS (PC/SS) systems [6]. In the PC/SS systems, multiple orthogonal sequences are simultaneously transmitted out of a pre-assigned orthogonal sequence set for a single user. Phase shift keying (PSK) is employed to specify the phase of individual transmitting orthogonal sequences. In other words, this is a partial-code-parallel [7] technique that includes orthogonal signaling DS/SS and all-code-parallel DS/SS [8] techniques as special cases.

The second point is how to maintain required error rate performances under severe channel conditions such as multipath fading. It is well known that forward error correction (FEC) coding is effective against noise, interference, jamming, fading, and other channel impairments. Meanwhile, interleaved serial and parallel concatenated codes [8], [9] with iterative decoding can offer a significant improvement in error rate performances. Key components of the improvements are an interleaver and iterative decoding with 'soft-in/soft-out' (SISO) decoder. Iterative demodulation/decoding, based on the idea of serial concatenated codes, has been a topic of recent interest [10]–[12]. In this decoding scheme, the modulator is considered as an inner code in a serial concatenated code scheme. This thought implements the iterative decoding strategy with just a single encoder, although two encoders are required in the iterative decoding of ordinary serial concatenated codes.

In the PC/SS systems, several FEC coding scheme have been investigated to implement a high-speed and low error rate system. As a block coding, Reed-Solomon coding has been applied in [13], [14]. On the other hand, convolutional coding with soft decision Viterbi decoding has been applied in [15]. In these coding schemes, iterative demodulation/decoding scheme has been not yet employed.

In this paper, an iterative demodulation/decoding scheme for coded PC/SS systems is proposed. We focus on a convolutional code as a channel code in this paper. The proposed demodulation/decoding scheme provides a capability of implementing high-speed and low-error rate data transmission systems with a simple structure of the transmitter.

To implement the iterative demodulation/decoding for the coded PC/SS systems, an SISO PC/SS demodulator based on an a posteriori probability (APP) algorithm is proposed. A PC/SS system uses a nonsystematic constant weight coding to select transmitting orthogonal PN sequences. Therefore, the PC/SS modulation can be consid-ered as a kind of block coding

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[†]The author is with the Graduate School of Science and Technology, Niigata University, Niigata-shi, 950-2181 Japan.
[††]The authors are with the Department of Electrical Engineering, Niigata University, Niigata-shi, 950-2181 Japan.
a) E-mail: takizawa@telecom0.eng.niigata-u.ac.jp

where binary bits are transformed to a PSK modulated constant weight codeword. We utilize this concept for the implementation of an SISO demodulator. In this paper, bit error rate (BER) performances on additive white Gaussian noise (AWGN) channel are evaluated by computer simulations.

In the next section, the concept of PC/SS systems and the system configurations of the PC/SS systems are de-scribed. In Sect. 3, an SISO PC/SS demodulator based on APP algorithm is proposed, and the iterative demodulation and decoding strategy is described in Sect. 4. Finally, simulation results on BER performance are shown under AWGN channel, and conclusions follow.

2. Configurations of the PC/SS Systems

In the PC/SS systems, a set of M orthogonal sequences is assigned for an individual user. Information data is conveyed by r orthogonal sequences that are chosen among M pre-assigned orthogonal sequences. Additional information data is conveyed by employing BPSK modulation for each orthogonal sequence to be transmitted. The amount of information bits per symbol is

$$K = \left\lfloor \log_2 \binom{M}{r} \right\rfloor + r \tag{1}$$

bits, where $\lfloor x \rfloor$ stands for the maximum integer that is less than or equal to x. The first term stands for the combination data of transmitting orthogonal sequences, and the second term stands for the phase data of those transmitting sequences.

A basic concept of PC/SS modulation is illustrated in Fig. 1. In this figure, we set $M = 8$, $r = 2$ and $K = 6$. Let

$$\mathbf{u} = \{u_1, ..., u_k, ..., u_K\}, \quad u_k \in \{0, 1\} \tag{2}$$

be the input information data. This data with K bits is divided into two parts: the first is the combination data, and the other is the phase data. The combination data is fed to a constant weight encoder with length M and Hamming weight r. For abbreviation, this constant weight codes will be referred to as (M, r)-CWC. r transmitting sequences are determined by choosing orthogonal sequences corresponding to '1' bits in a CWC codeword. The phase data is fed to a BPSK modulator to determine the phase of transmitting orthogonal sequences. Let

$$\mathbf{x} = \{x_1, ..., x_j, ..., x_M\}, \quad x_j \in \{-1, 0, +1\} \tag{3}$$

be the transmitted codeword, and it is called as a modulated CWC codeword. This codeword is transmitted as a signal that is the sum of the r BPSK modulated orthogonal PN sequences.

In the receiver, a received signal is fed to a bank of M correlators. Let

$$\mathbf{z} = \{z_1, ..., z_j, ..., z_M\}, \quad z_j \in \Re \tag{4}$$

denote the correlator outputs. Conventional maximum likelihood (ML) demodulation in the PC/SS systems is illustrated in Fig. 2. This estimation result forms a (M, r)-modulated CWC $\hat{\mathbf{x}}$ in such a way that r bits corresponding to the transmitted orthogonal sequences are '+1' or '−1' and remaining $M - r$ bits are '0,' where the sign of '1' is the same as the sign of the correlator output. The constant weight decoder decodes the absolute value of (M, r)-modulated CWC estimate $|\hat{\mathbf{x}}|$ for combination data. Another information to be demodulated is the phase data of transmitted sequences. Based on the previous estimation of the transmitted orthogonal sequence combination, r correlator outputs are selected among M outputs of the correlator bank. The selected correlator outputs are fed to BPSK demodulators in parallel and are demodulated to the phase data. Then the estimation of the information data $\hat{\mathbf{u}}$ is decided.

3. PC/SS Demodulation Based on a Posteriori Probability Algorithm

The ML demodulator described in the previous section is considered as a 'soft-in/hard-out' demodulator because it gives only hard estimates. However, an SISO PC/SS demodulator is necessary to implement the iterative demodulation/decoding. In this section, a trellis

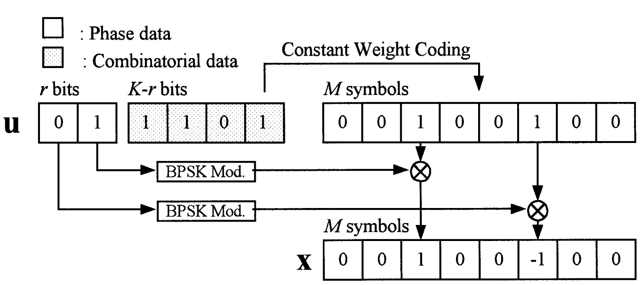


Fig. 1 Basic concept of PC/SS modulation by employing (M, r)-CWC. $M = 8$, $r = 2$ and $K = 6$.

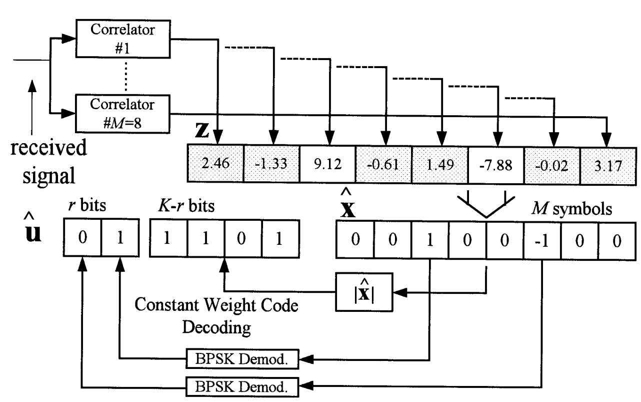


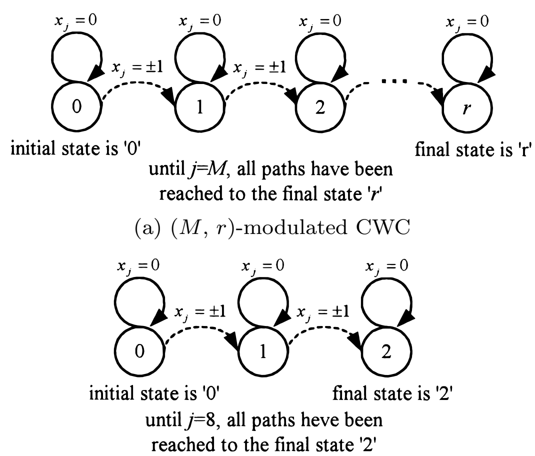
Fig. 2 PC/SS demodulation based on ML criterion. $M = 8$, $r = 2$ and $K = 6$.

diagram for modulated CWC is defined and an SISO PC/SS demodulator is presented based on APP algorithm.

3.1 Definition of a Trellis Diagram for Modulated CWC

Since CWC is a nonsystematic code, the APP decoding algorithm for systematic codes [8] cannot be applied directly. At first, we need to define the trellis diagram of modulated CWC. In this code, the Hamming weight of all codewords is constant, that is r in (M, r)-modulated CWC. The state diagram for (M, r)-modulated CWC is displayed in Fig. 3(a). This state diagram has $r+1$ states. Each state indicates the Hamming weight in a part of a codeword from the element x_1 to the element x_j, and all paths reach to the 'state r' until j comes to M. As an example, the state diagram for (8, 2)-CWC is displayed in Fig. 3(b). In this example, the number of states is three. All paths run from 'state 0' at j=0 to 'state 2' at j=8. The trellis diagram for this state diagram is shown in Fig. 4. A branch in this trellis diagram is labeled by a modulated CWC coded bit, x_j. A path leaves the initial state, 'state 0,' and reaches to the final state, 'state 2,' until j=8. In an (M, r)-modulated CWC, all paths reach the final state, 'state r,' until j=M.

The transition probability (or the branch metric)



(a) (M, r)-modulated CWC

(b) (8, 2)-modulated CWC

Fig. 3 State diagram for a modulated CWC.

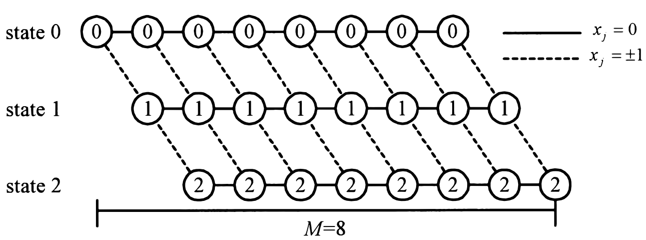


Fig. 4 Trellis diagram for (8, 2)-modulated CWC.

from state s' to state s at j, $\gamma_j(s', s)$, is computed as

$$\begin{aligned}\gamma_j(s', s) &= p(z_j|s', s) \cdot P(s|s') \\ &= p(z_j|x_j) \cdot P(x_j)\end{aligned} \tag{5}$$

where $P(x_j)$ is the a priori probability for the coded bit, x_j, and $p(z_j|x_j)$ is the conditional probability for the jth correlator output z_j conditioned on x_j. If AWGN channel is assumed, $p(z_j|x_j)$ is given by

$$p(z_j|x_j) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left\{ -\frac{(z_j - x_j)^2}{2\sigma^2} \right\} \tag{6}$$

In Eq. (6), the noise variance σ^2 is determined by the signal-to-noise ratio (SNR) per bit E_b/N_0, the coding rate R_c and some PC/SS parameters:

$$\sigma^2 = \frac{1}{R_c \cdot E_b/N_0 \cdot K/r} \tag{7}$$

3.2 PC/SS Demodulator Based on APP Algorithm

In the transmitter of a PC/SS system illustrated in Fig. 5, a block of information bits $\mathbf{u}$ is modulated and transmitted as a modulated CWC codeword $\mathbf{x}$. In the receiver, the received codeword $\mathbf{z}$ is obtained as a set of outputs from a bank of M correlators.

In an SISO PC/SS demodulator illustrated in Fig. 6, two inputs are of the form of probabilities. On the other hand, two outputs are of the form of log likelihood ratios. One output is a posteriori information defined by

$$L(\hat{u}_k) \equiv L(u_k|\mathbf{z}) = \log \frac{P(u_k = 1|\mathbf{z})}{P(u_k = 0|\mathbf{z})} \tag{8}$$

where k is time index, k=1, ..., K. The other output is extrinsic information that is computed by subtracting the input component influencing on u_k from a posteriori probability. Channel information can be obtained from the product of the conditional probability.

$$p_{ch}(\mathbf{z}|\mathbf{x}) = \prod_{j=1}^{M} p(z_j|x_j) \tag{9}$$

Equation (8) can be written as [8]

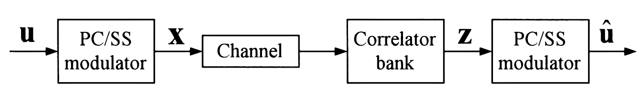


Fig. 5 Block diagram of a PC/SS system.

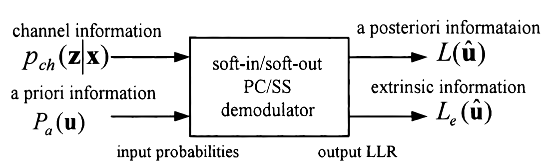


Fig. 6 SISO PC/SS demodulator.

$$L(\hat{u}_k) = \log \frac{\displaystyle\sum_{u_k=1, x\in C_{pc}} P(\mathbf{x}|\mathbf{z})}{\displaystyle\sum_{u_k=0, x\in C_{pc}} P(\mathbf{x}|\mathbf{z})} = \log \frac{\displaystyle\sum_{u_k=1, x\in C_{pc}} p_{ch}(\mathbf{x}|\mathbf{z})P(\mathbf{x})}{\displaystyle\sum_{u_k=0, x\in C_{pc}} p_{ch}(\mathbf{x}|\mathbf{z})P(\mathbf{x})} \quad (10)$$

where C_{pc} stands for the set of all modulated CWC codewords. The probability of $P(\mathbf{x}|\mathbf{z})$ in Eq. (10) can be computed by the channel information $p_{ch}(\mathbf{z}|\mathbf{x})$ and a priori probability $P(\mathbf{x})$ that is a priori probability for a modulated CWC codeword $\mathbf{x}$ and is unknown at the receiver. Fortunately, an SISO PC/SS demodulator can utilize as a priori probability for the demodulated bits $\mathbf{u}$. In addition, $P(\mathbf{x})$ is replaced by $P_a(\mathbf{u})$ because of a one-to-one correspondence between $\mathbf{x}$ and $\mathbf{u}$. That is,

$$P(\mathbf{x}) = P(\mathbf{u}) = \prod_{k=1}^{K} P_a(u_k) \quad (11)$$

where

$$\mathbf{u} = C_{pc}^{-1}(\mathbf{x}) = \{u_1, u_2, ..., u_K\} \quad (12)$$

This conversion enable us to compute the a posteriori probability in Eq. (8), also to implement an SISO PC/SS demodulation.

The extrinsic information $L_e(\hat{u}_k)$ is given by

$$L_e(\hat{u}_k) = L(\hat{u}_k) - L_a(u_k) - L_{ch}(u_k) \quad (13)$$

where $L_a(u_k)$ is a priori information in log likelihood ratio.

$$L_a(u_k) = \log \frac{P_a(u_k = 1)}{P_a(u_k = 0)} \quad (14)$$

$L_{ch}(u_k)$ is computed by using the one-to-one correspondence between $\mathbf{u}$ and $\mathbf{x}$ as follows.

$$L_{ch}(u_k) \equiv \log \frac{p(u_k = 1|\mathbf{z})}{p(u_k = 0|\mathbf{z})} = \log \frac{\displaystyle\sum_{u_k=1, x\in C_{pc}} p(\mathbf{x}|\mathbf{z})}{\displaystyle\sum_{u_k=0, x\in C_{pc}} p(\mathbf{x}|\mathbf{z})} \quad (15)$$

Bit error rate (BER) performance in PC/SS systems with this APP demodulator is displayed in Fig. 7. The specifications on this simulation are shown in Table 1. The results are obtained by computer simulations. The upper bound on the ML demodulation is also plotted in this figure. If the number of transmitting sequences increases, the number of information bits per symbol also increases. However, BER performance gradually degrades because the signal power per transmitting sequence decreases.

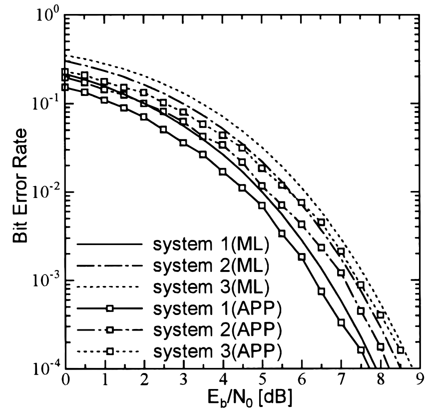


Fig. 7 BER comparison between APP PC/SS demodulator and ML PC/SS demodulator.

Table 1 Specifications of the PC/SS for comparison.

	system 1	system 2	system 3
# of assigned sequences	$M = 8$		
# of transmitting sequences	$r = 2$	$r = 3$	$r = 4$
transmitting bits per symbol	$K = 6$	$K = 8$	$K = 10$
constant weight coding	Shalkwijk's CWC [16]		
Orthogonal sequences	Walsh-Hadamard code		

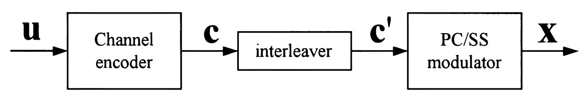


Fig. 8 Channel coded PC/SS system.

4. Iterative Demodulation and Decoding for Coded PC/SS Systems

In this section, we introduce an implementation of the iterative demodulation/decoding for channel coded PC/SS systems by using an SISO PC/SS demodulator described in the previous section.

The block diagram of a coded PC/SS transmitter model is shown in Fig. 8. This system consists of an arbitrary channel encoder, a random interleaver, and the PC/SS modulator. The interleaver permutes the codewords $\mathbf{c}$, and generate a permuted codeword $\mathbf{c}'$. The main role of the interleaver in the systems is to construct long code from a simple short code [17]. In this paper, a uniform random interleaver is employed. This interleaver brings average performance among the set of all interleavers [9]. The PC/SS modulator transform the permuted codeword $\mathbf{c}'$ into a CWC codeword $\mathbf{x}$.

Figure 9 illustrates the block diagram of the iterative demodulation and decoding process. In the receiver, the received signal passes through a correlator bank to obtain a set of correlator outputs. These correlator outputs are considered as the received codeword $\mathbf{z}$ for the transmitted codeword $\mathbf{x}$.

Channel information $p_{ch}(\mathbf{z}|\mathbf{x})$ computed by Eq. (9)

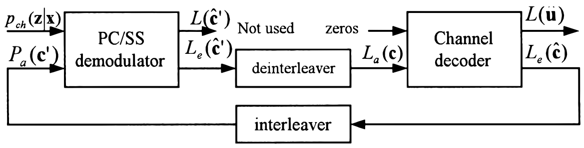


Fig. 9 Block diagram for the iterative demodulation/decoding process.

is fed to the iterative demodulation and decoding process. The initial a priori information for the PC/SS demodulator $P_a(\mathbf{c}')$ is set to one half. Only the output $L_e(\hat{\mathbf{c}})$ is provided to the channel decoder through an interleaver.

In the channel decoder, a posteriori information $L(\hat{\mathbf{u}})$ and extrinsic information $L_e(\hat{\mathbf{c}})$ are computed based on the APP algorithm. $L_e(\hat{\mathbf{c}})$ is fed back to the PC/SS demodulator as a priori information $P_a(\mathbf{c}')$ for the PC/SS demodulator via the interleaver. From a priori information $L_a(\mathbf{c}')$, each element of $P_a(\mathbf{c}')$ is computed by

$$P_a(c'_j) = \begin{cases} \dfrac{e^{L_a(c'_j)}}{1+e^{L_a(c'_j)}} & (\text{for } c'_j = 1) \\ \dfrac{1}{1+e^{L_a(c'_j)}} & (\text{for } c'_j = 0) \end{cases} \tag{16}$$

The iterative demodulation and decoding process completes by using this probability as a priori information in the PC/SS demodulator. After iterations, the decoder make a hard decision on $\mathbf{u}$ based on $L(\hat{\mathbf{u}})$.

5. Simulation Results

BER performance in the coded PC/SS systems with proposed iterative decoding/demodulation is evaluated by computer simulations. A half rate nonsystematic convolutional code with generator $G = [5, 7]$ in an octal form is applied as a channel code. AWGN channels are assumed. It is also assumed that the variance of noise is known at receivers.

5.1 Effect of the Number of Iterations

Table 1 lists the specifications of the PC/SS parameters in this simulation. Figure 10 displays BER performance versus signal-to-noise ratio per bit, E_b/N_0, in system 1. Interleaver size is set to 1200. BER performance is improved dramatically as the number of iterations increases. However, this BER improvement diminishes when the number of iterations becomes larger. After five iterations, required E_b/N_0 for BER of 10^{-5} becomes 3 dB that is lower by 5.5 dB than that in the uncoded system 1.

Note that an error floor is observed in above 3.0 dB in 4 or 5 iterations. This phenomenon is caused by the small minimum distance of the modulated CWC. For example, in PC/SS system 1, the minimum distance of

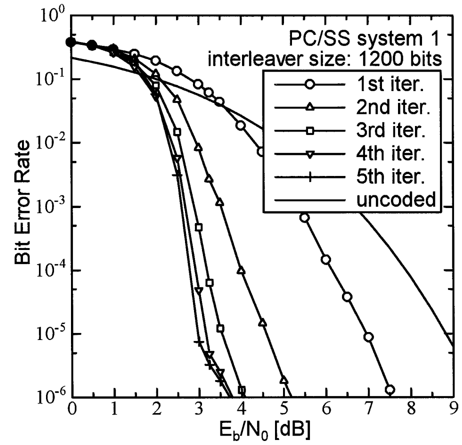


Fig. 10 BER performance of convolutional coded system 1, in various number of iterations.

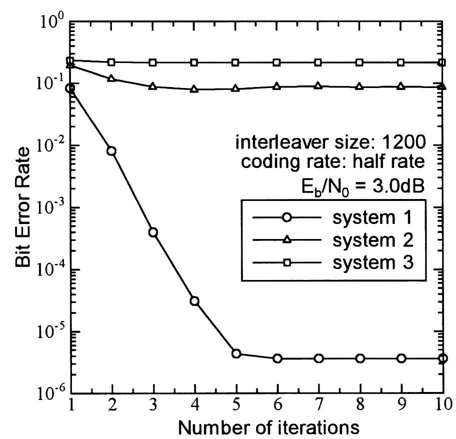


Fig. 11 BER performance of coded systems versus the number of iterations.

the output codeword from the PC/SS modulator is only two. Figure 11 displays BER performances versus the number of iterations in system 1, system 2, and system 3. E_b/N_0 is set to 3.0 dB. The improvement in BER grows linearly in each system at first three iterations. However, the returns gradually diminish as the number of iterations is increased.

5.2 Effect of Interleaver Size

Figure 12 displays the BER performances in system 1 for various sizes of a random interleaver. The number of iterations is set to five. Clearly, the performance is improved as the increase in the interleaver size. The coding gain in serial and parallel concatenated code depends on its interleaver size [9]. These results demonstrate that the interleaver gain is obtained in the coded PC/SS system just like in serial concatenated block codes [9].

An expansion of the interleaver size brings some improvements in the error rate performance. However, the expansion of the interleaver size causes a large delay

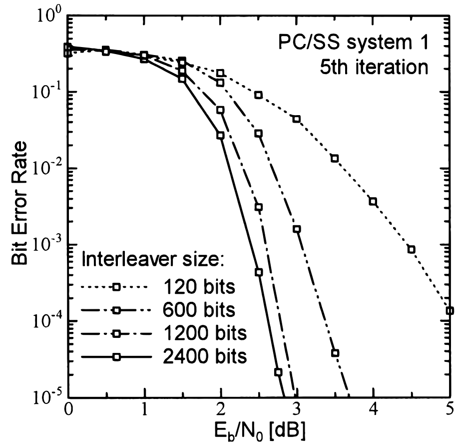


Fig. 12 Comparison for different interleaver size.

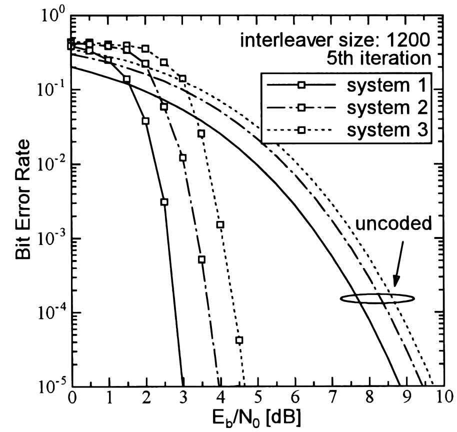


Fig. 14 BER performance for convolutional coded system 1, system 2, and system 3.

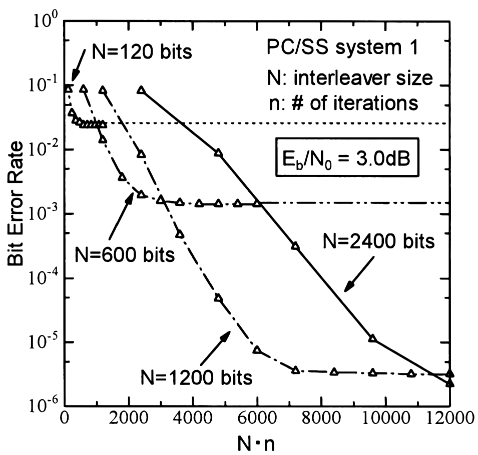


Fig. 13 BER performance versus $N \cdot n$ for several interleaver sizes.

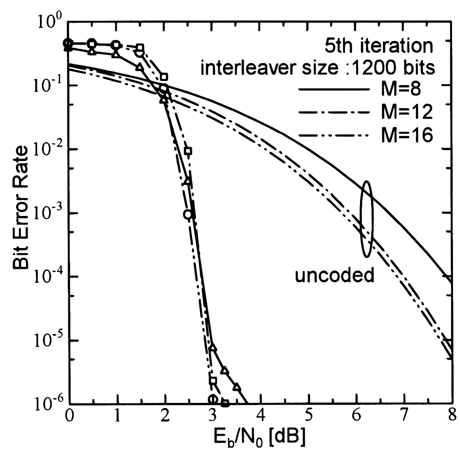


Fig. 15 BER performances for the various numbers of the assigned sequences.

for the decoding processing. Figure 13 displays the bit error rate performance versus the product of the number of iterations n and the interleaver size N. The delay for the decoding processing increase linearly for the growth of the product of $n{\cdot}N$. Figure 13 suggests that if the interleaver size is small, low error rate such as 10^{-5} in BER is not achievable. Therefore, a sufficient interleaver length is required to maintain a low error rate performance. On the other hand, suppose that the target BER is set to 10^{-5}. In this figure, the system with 1200 bits interleaver achieves the target BER, and also the system with 2400 bit-interleaver does it. However, the 2400 bit-interleaver system costs about 1.5 times larger delay than the 1200 bit-interleaver system.

5.3 Effect of the Number of Transmitting Sequences and Assigned Sequences

If the number of transmitting sequences is increased in PC/SS systems, more information bits are conveyed. In Fig. 14, BER performances for system 1, system 2, and system 3 are shown. The number of iterations is set to five. The interleaver size is 1200 bits. The required E_b/N_0 for 10^{-5} in BER are 4 dB and 4.5 dB in system 2 and system 3, respectively. Those values are lower by 5.5 dB and 5 dB than that in the uncoded system 2 and system 3, respectively. As shown in two plots for system 1, the coding gain is 5.5 dB. However, coding gain gradually diminishes as the number of transmitting sequences is increased. Figure 15 displays BER performances of system 1. The number of the assigned orthogonal PN sequences M takes three values, 8,12 and 16. The number of transmitting sequences is constant and is set to two, and the number of the information bits K is 6, 8 and 8 bits in M of 8, 12 and 16, respectively. The required E_b/N_0 to maintain 10^{-5} in BER is almost same in each system. However, the error floor in M=8 is observed in the least E_b/N_0.

5.4 Effect of Puncturing Operations

Puncturing the encoder output is a popular method to increase the total coding rate in convolutional coding.

Table 2 Puncturing pattern for a half rate convolutional code.

Coding rate	Puncturing pattern
2/3	$\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$
3/4	$\begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$
4/5	$\begin{bmatrix} 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 \end{bmatrix}$

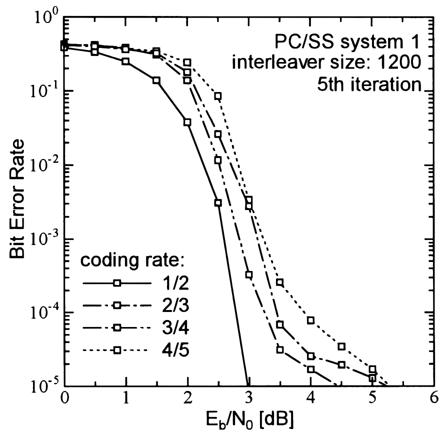


Fig. 16 Comparison for different coding rate by puncturing operation.

Table 3 Comparison of the information bit rate.

PC/SS system	coding rate R_c	# of transmitting information bits K	# of information bits per symbol
system 1	1/2	6	3
system 1	2/3	6	4
system 1	3/4	6	4.5
system 1	4/5	6	4.8
system 2	1/2	8	4
system 3	1/2	10	5

This is another approach to increase the information bit rate in convolutional coded PC/SS systems. The puncturing pattern P is shown in Table 2. Figure 16 shows the effect of puncturing operations in the coded system, system 1, with five time-iterative demodulation/decoding. Interleaver size is again 1200. BER floor appears, especially at higher coding rates. When the coding rate is 4/5, error floor is observed beyond 10^{-5} in BER in spite of five time-iterative demodulation/decoding in the receiver. Table 3 shows the number of transmitting information bits per symbol. Consider the half-rate coded PC/SS system 2 and punctured 2/3-rate coded PC/SS system 1. Figure 17 shows BER performances of these systems. Both systems have the same information bit rate. The latter system shows slightly better BER performance than the former system if E_b/N_0 is lower than 4 dB. On the contrary, BER in the latter system exceeds that in the for-mer system if E_b/N_0 stays beyond 4 dB, because the error floor appears around 10^{-5} BER.

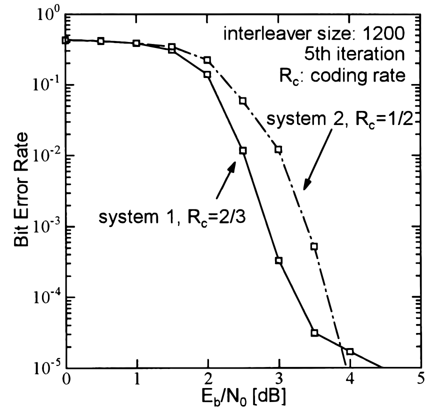


Fig. 17 BER comparison between system 1 and system 2.

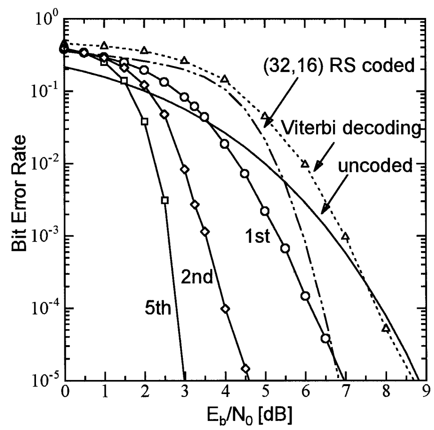


Fig. 18 Comparison with different coding and decoding methods.

5.5 Comparison with Other Coding and Decoding Scheme

Figure 18 displays the comparison in BER performance with other channel coding and decoding methods for system 1. BER performances in the Reed Solomon coded PC/SS system [13] and in the convolutional coded PC/SS system with hard decision-Viterbi decoding are plotted. In the Reed Solomon coded system, (32,16) half rate-Reed Solomon coding on GF(2^6) is applied, and we compute the BER performance theoretically in the assumption of a bounded distance decoding. In the convolutional coded system, the applied convolutional code is the same as the code in iterative demodulation/decoding that is nonsystematic code with generator G=[5, 7]. In both systems, an ML demodulator presented in Sect. 2 is used as the PC/SS demodulator.

In the comparison between the iterative demodulation/decoding method and the Reed Solomon coding method, the performance of the proposed method after the second iteration is superior to Reed Solomon coding method in required E_b/N_0 satisfied with 10^{-5} BER.

After the fifth iteration, the coding gain becomes more than 3.5 dB.

The performance of the convolutional coded system is inferior to both the Reed Solomon coding method and the iterative method. The reason for this result owes the natural properties of PC/SS systems: since several bits are transmitted by a single symbol, symbol-based FEC such as Reed Solomon codes is more qualified than bit-based FEC such as convolutional codes, BCH codes, etc. [13]. After the fifth iteration, coding gain is about 5.5 dB in required E_b/N_0 to satisfy the BER of 10^{-5}.

6. Conclusions

We have applied an iterative demodulation and decoding scheme to coded PC/SS systems to improve the error rate performance. To implement this decoding scheme, we have proposed an SISO PC/SS demodulator based on APP algorithm. Simulation results show that this iterative demodulation and decoding offers a significant improvement in the error rate performance. Larger interleaver gain is obtained when interleaver size increases.

We have two options to increase the information data rate. One is increasing the number of transmitting se-quences, and the other is applying a puncturing operation in convolutional code. The former system is better than the latter system in lower BER such as 10^{-5}, because the error floor appears at larger BER in the latter system when the total information bit rate are identical.

Investigation of the channel capacity for the proposed systems is one of the important problems. High-speed data transmission is the most significant performance of the PC/SS systems, and the investigation will indicate the performance effectively. This will be a future work.

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Ken-ichi Takizawa was born in Niigata, Japan, in 1975. He received B.E. and M.E. degrees from Niigata University, Niigata, in 1998 and 2000, respectively. He is currently a Ph.D. candidate at Graduate School of Science and Technology, Niigata University. His research interests include digital wireless communications and channel coding. He is a student member of IEEE.

Shigenobu Sasaki was born in Nara, Japan on April 18, 1964. He received B.E., M.E. and Ph.D. degrees from Nagaoka University of Technology in 1987, 1989 and 1993, respectively. Since 1992, he has been with the Department of Electrical and Electronic Engineering, Niigata University. Currently he is an Associate Professor in the same department. During a year of 1999 to 2000, he was a visiting scholar at the Department of Electrical and Computer Engineering, University of California, San Diego. His research interests are in the area of digital communications with special emphasis on spread spectrum communication systems, and digital signal processing. He is a member of IEEE and SITA.

Shogo Muramatsu was born in Tokyo, Japan in 1970. He received B.E., M.E. and Dr.Eng. degrees in electrical engineering from Tokyo Metropolitan University in 1993, 1995 and 1998, respectively. In 1997, he joined Tokyo Metropolitan University. In 1999, he joined Niigata University, where he is currently an Associate Professor at the Department of Electrical and Electronic Engineering. His research interests are in digital signal processing, multirate systems, image processing and VLSI architecture. He is a Member of IEEE.

Hisakazu Kikuchi was born in Niigata, Japan, in 1952. He received B.E. and M.E. degrees from Niigata University, Niigata, in 1974 and 1976, respectively, and Dr. Eng. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, in 1988. From 1976 to 1979 he worked at Information Systems Laboratories, Fujitsu Ltd. Since 1979 he has been with Niigata University, where he is a Professor in electrical engineering. During a year of 1992 to 1993, he was a visiting scientist at the Electrical Engineering Department, University of California, Los Angeles. His research interests include digital signal processing, image processing, wavelets, and mobile telecommunications. He is a member of IEEE, Institute of Image Information and Television Engineers, and Japan SIAM.