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Memory Access Estimation of Filter Bank Implementation on Different DSP Architectures

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SUMMARY A unified polyphase representation of analysis and synthesis filter banks is introduced in this paper, and then the efficient implementation on digital signal processors (DSP) is investigated. Especially, the number of memory accesses, power consumption, processing accuracy and the required instruction cycles are discussed. Firstly, a unified representation is given, and then two types of procedures, SIMO system-based and MISO system-based procedures, are shown, where SIMO and MISO are abbreviations for single-input/multiple-output and multiple-input/single-output, respectively. These procedures are compared to each other. It is shown that the number of data load in SIMO system-based procedure is a half of that in MISO system-based procedure for two-channel filter banks. The implementation of M-channel filter banks is also discussed.

key words: *digital signal processor (DSP), filter banks, wavelet transforms, multiplier and accumulator (MAC)*

1. Introduction

Image coding techniques are indispensable for efficient use of transmission channel and media in the area of digital image communication and storage. The new standards JPEG 2000 for still image coding and MPEG-4 for video coding employ the wavelet transform technique [1]. The wavelet transform is known to have a tree structure of two-channel filter banks [2], [3]. On the other hand, M-channel filter banks are also expected to be applied to image and video coding as a subband coding (SBC) technique [4]. Thus, the efficient implementation of filter banks is of quite interest.

When implementing WTC or SBC systems, a programmable DSP is superior to a dedicated VLSI in terms of flexibility, while keeping high performance. Programmable DSPs have several different architectures such as accumulator-based and VLIW (Very Long Instruction Words) architectures [5]. Multiply-and-accumulator (MAC) unit is one of the main features of accumulator-based DSPs. Even though the MAC units are only considered, there exist a lot of different architectures, for example, in terms of the number of MAC units and the number of accumulators. In addition, the processing procedure itself is strongly related to the efficiency of memory access, the processing accuracy and so forth. The redundant memory access is known to affect the power consumption [6].

This paper introduces a unified polyphase representation of analysis and synthesis filter banks, and then considers the efficient implementation on accumulator-based DSPs. Efficiency will be discussed in terms of memory access, power consumption and processing accuracy. This paper supposes several accumulator-based DSP architectures. Regarding the memory access, we also define two types of procedures: SIMO system-based and MISO system-based procedures. The main purpose of this work is to compare these procedures on different DSP architectures.

The organization of this paper is as follows. As a preliminary, in Sect. 2, filter banks are reviewed. In Sect. 3, DSP architectures are discussed. In Sect. 4, the memory access is estimated for two-channel filter bank implementation. Implementations of M-channel filter banks are also discussed in Sect. 5, and conclusions follow in Sect. 6.

2. Review of Filter Banks

In this section, as a preliminary, we briefly review filter banks. Firstly, the parallel structure is explained. Then, the polyphase representation is shown. In order to deal with both of analysis and synthesis banks equivalently, we introduce a unified polyphase representation.

2.1 M-Channel Filter Banks

Figure 1(a) shows a parallel structure of M-channel maximally decimated filter banks [2], [3], where $H_k(z)$ and $F_k(z)$ are the analysis and synthesis filters, respectively. $Y_k(z)$ denotes the k-th subband signal. The boxes including $\downarrow M$ and $\uparrow M$ denote the downsampler and upsampler with the factor M, respectively.

The structure shown in Fig. 1(a) can always be rewritten in terms of polyphase matrices as shown in Fig. 1(b), where $\mathbf{E}(z)$ and $\mathbf{R}(z)$ denote the $M \times M$ polyphase matrices corresponding to the analysis and synthesis banks, respectively [3].

2.2 Unified Polyphase Representation

In order to deal with both of analysis and synthesis

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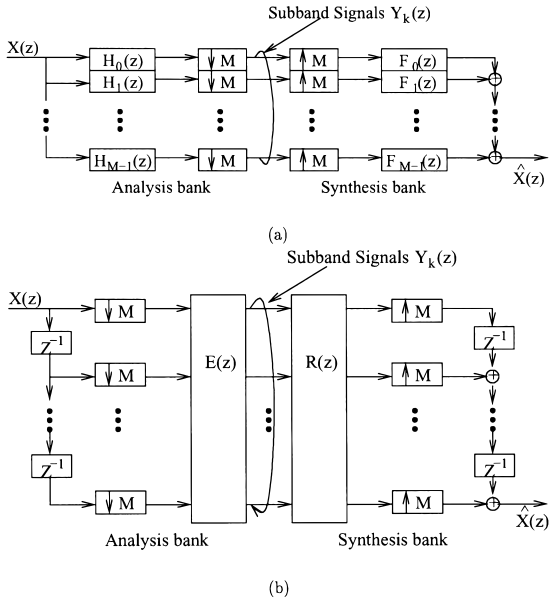

Fig. 1 M-channel maximally decimated filter banks.

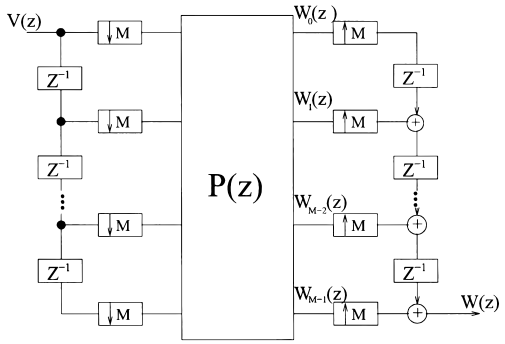

Fig. 2 Unified polyphase representation. For an analysis bank, $\mathbf{P}(z) = \mathbf{E}(z)$. For a synthesis bank, $\mathbf{P}(z) = \mathbf{R}(z)$.

banks equivalently, we present a unified polyphase representation. Figure 2 shows the unified polyphase representation [7], where $\mathbf{P}(z)$ is either of $\mathbf{E}(z)$ or $\mathbf{R}(z)$ in Fig. 1(b). In other words, it can behave as both analysis and synthesis banks. The unified polyphase representation is provided on the assumption that the subband signals $Y_k(z)$ are interleaved each other so that the sampling frequency rates of input $V(z)$ and output $W(z)$ become the same.

The signals $X(z)$, $Y_k(z)$ and $\hat{X}(z)$ in Fig. 1 relate to $V(z)$ and $W(z)$ in Fig. 2 as follows:

For the analysis bank,

$$V(z) = X(z), \tag{1a}$$

$$W(z) = \sum_{k=0}^{M-1} Y_{M-1-k}(z^M) z^{-k}. \tag{1b}$$

For the synthesis bank,

$$V(z) = z^{-M} \sum_{k=0}^{M-1} Y_k(z^M) z^{-k}, \tag{2a}$$

$$W(z) = z^{-1} \hat{X}(z). \tag{2b}$$

Although, from Eq. (2b), there is one delay for the output signal $\hat{X}(z)$, the difference between analysis and synthesis banks become out of question. Furthermore, for a DSP implementation, where the number of resources is limited, this representation has the following advantages:

- The whole system can be regarded as a single-input single-output system.
- The input and output sampling rates are identical to each other.
- Since it is based on the polyphase representation, redundant operations are eliminated.
- Program modules for analysis and synthesis banks become the same with each other.

It is none other than clarifying the memory access procedure for subband signals. Note that the serial/parallel converter, that is the delay chain with downsamplers, and the parallel/serial converter, that is the delay chain with upsamplers, influence only the addressing for reading $V(z)$ and writing $W(z)$, respectively. Operations are not affected.

2.3 Two Types of Procedures

This paper refers to a procedure as the order of memory accessing for the polyphase filtering, which relates to the resource binding and timing scheduling on DSPs. The procedure for the implementation of filter banks as shown in Fig. 2 is not unique. The choice influences the efficiency, for example, memory access, the power consumption, processing accuracy and so forth. For the latter discussion, we show two types of procedures. One is based on multi-input-single-output (MISO) systems as shown in Fig. 3, and the other is based on single-input-multi-output (SIMO) systems as shown in Fig. 4.

Figure 3(a) is rewritten from Fig. 2. Figure 3(b) shows the structure of the k-th MISO system, where $\mathbf{P}_k^{(1\times M)}(z) = [P_{k,0}(z), P_{k,1}(z), \ldots, P_{k,M-1}]$ and $P_{k\ell}(z)$ denotes the k,ℓ-th element of $\mathbf{P}(z)$. Similarly, Fig. 4(a) is rewritten from Fig. 2. Figure 4(b) shows the structure of the l-th SIMO system, where $\mathbf{P}_l^{(M\times 1)}(z) = [P_{0,l}(z), P_{1,l}(z), \ldots, P_{M-1,l}]^T$. These representations imply that the procedure of read and write data is not unique when the system is implemented on some DSP. Note that, however, the number of operations is independent of the way of representation.

The purpose of this paper is to investigate what kind of procedure is proper for a provided processor in terms of memory access.

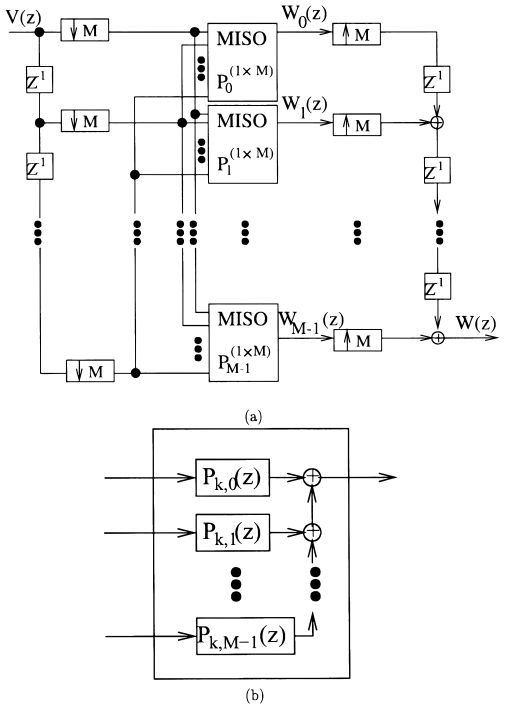

Fig. 3 MISO system-based representation.

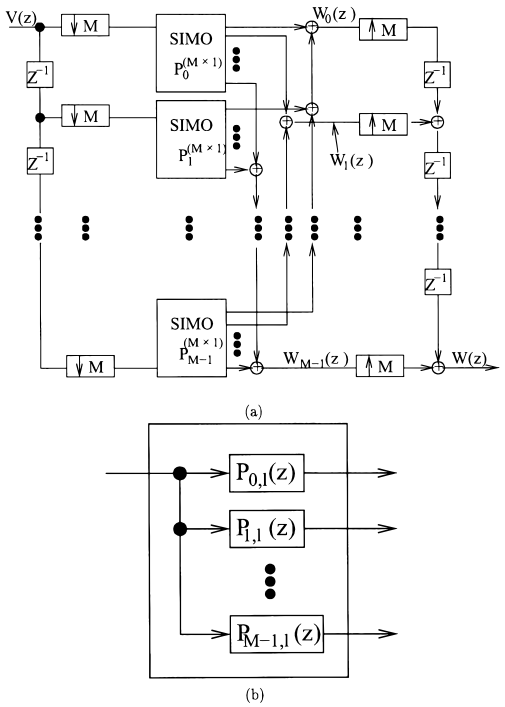

Fig. 4 SIMO system-based representation.

3. Architectures with Multiple MAC Units

In general, the functional units of a DSP are a collection of ALUs, MAC units, barrel shifters, data/program buses, on-chip memories for data and programs and other special operation units. In order to offer higher parallelism in instructions and higher throughput rate in data streams, the Harvard architecture is widely used, where the control circuit is assembled by splitting the memory space into two separate areas for data and programs. The address generation unit usually controls more than two pointers.

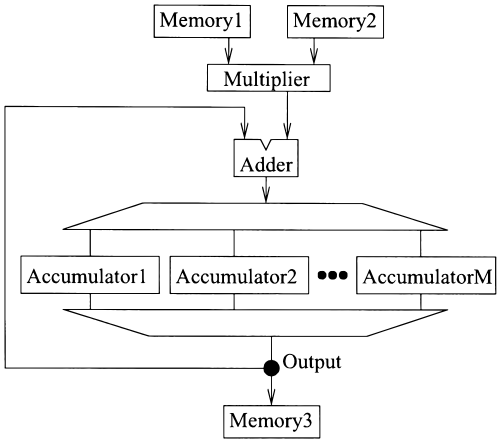

Fig. 5 Multi-Accumulator MAC unit.

Even with respect to the functional units in a category of the Harvard architecture, there exist a number of different architectures. A typical DSP has a single accumulator in its MAC unit. On the other hand, some recent DSPs such as TMS320C54x are equipped with multiple accumulators in their MAC units. Figure 5 shows a MAC unit with multiple accumulators.

In this section, several assumptions and constraints are given for latter discussion to find a better procedure of filter bank implementation on some DSPs of different architectures.

3.1 Assumptions

The performance of a DSP is mainly determined by the memory access as well as the number of operations [5], [6]. In order to estimate the memory access and other performance, we make some assumptions on the architecture as follows:

- Operations are in fixed-point arithmetic.
- Data buses do not encounter any collisions.
- A single MAC operation completes in a single instruction cycle.
- All operations at different MAC units are executed in parallel.
- Accumulators have enough length to prevent them from overflow and underflow.
- A single data word to be used in multiple MAC units at a specific time instance is fed to those units simultaneously.

TMS320C54x and TMS320C55x from Texas Instruments [8] are similar to DSPs on these assumptions.

In addition, we also consider the case that the address generator possesses a function of multi-cycle increment while repeating MAC instructions for the sake of simplification.

3.2 Processing Speed

For reference, let us estimate the required processing speed. An entire system shown in Fig. 2 involves a total number of operations per sample as follows:

$$n_{\mathrm{OP/SAMP}} = 2\{M(N+1)-1\}, \tag{3}$$

where N is the order of polyphase filters. Thus, the number of operations per second must satisfy $n_{\mathrm{OP/SEC}} \geq 2\{M(N+1)-1)\}F_{\mathrm{S}}$, where F_{S} is the sampling frequency of input and output sequences.

A DSP of interest is assumed to incorporate K MAC units. Since a single MAC instruction executes two operations of multiplication and addition, the number of operations per instruction cycle is

$$n_{\mathrm{OP/INS}} = 2K, \tag{4}$$

where the instruction cycle means a unit time of executing an instruction. As a result, the number of instructions per second $n_{\mathrm{INS/SEC}}$ is thus given by

$$n_{\mathrm{INS/SEC}} \geq \{M(N+1)-1\}F_{\mathrm{S}}/K. \tag{5}$$

This implies that

$$F_{\mathrm{clk}} \geq \{M(N+1)-1\}F_{\mathrm{S}}/K, \tag{6}$$

where F_{clk} is the clock frequency of a provided DSP.

4. Memory Access Estimation

The purpose of this section is to investigate what kind of procedure is proper for a provided DSP in terms of memory access. In this section, the memory access is estimated for several DSPs. Let us discuss the number of memory accesses and then the following things:

- Power consumption
- Processing accuracy
- Required instruction cycles

4.1 Implementation of Filter Banks

To count the number of memory accesses, SIMO and MISO system-based procedure are shown in detail. Although we discuss two-channel filter banks, the most statements are applicable to the M-channel case. Let us consider a MAC unit with one accumulator and a MAC unit with two accumulators. In addition, let us deal with the cases of single MAC unit and dual MAC units.

Figures 6(a) and (b) show the MISO system-based and SIMO system-based representations, respectively, where $P_{0,0}(z), P_{0,1}(z), P_{1,0}(z)$ and $P_{1,1}(z)$ are the elements of the polyphase matrix $\mathbf{P}(z)$.

In order to explain the procedure for a provided DSP, let us define a simplified instruction set as shown in Table 1, where ACC denotes an accumulator, $SRC0$ and $SRC1$ are data sources and DST is a destination. In this work, the following notations are used:

\# : Immediate value.
|| : Parallel instruction.
`(REG)` : The content of a register `REG`.
`(REG)+` : The content of a register `REG` with increment.
`(REG){+}` : The content of a register `REG` with increment of every two instructions.
`A,B,C,D` : Accumulators.
$\mathtt{RS}_n$: The register containing the address of $V_n(z)$ in

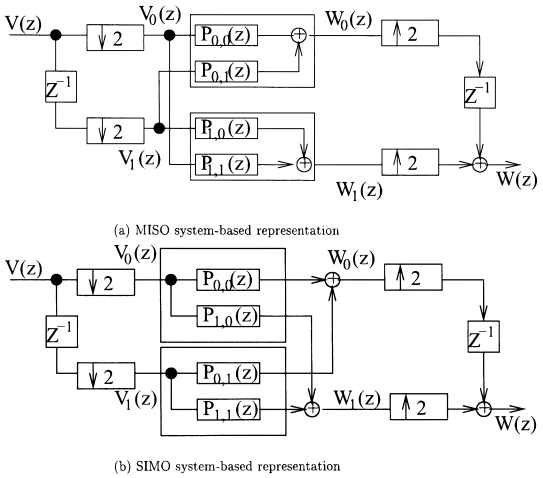

Fig. 6 Two types of representations for a two-channel filter bank.

Table 1 Simplified instruction set.

Instruction	Operand	Execution
CLR	ACC	$ACC \leftarrow 0$
MAC	$SRC0$,$SRC1$,ACC	$ACC \leftarrow ACC + (SRC0 \times SRC1)$
ADD	$SRC0$,$SRC1$,DST	$DST \leftarrow SRC0 + SRC1$
LD	SRC,DST	$DST \leftarrow SRC$
ST	SRC,DST	$SRC \rightarrow DST$
RPT	$\#N$	Repeat the following instruction $N+1$ times.
BRPT	$LABEL$	Repeat from the following instruction to $LABEL$ `BRC` times

```
CLR  A
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC0)+, A
RPT  #N
MAC  (RS1)+, (RC1)+, A
ST   A, (RD0)+
CLR  A
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC2)+, A
RPT  #N
MAC  (RS1)+, (RC3)+, A
ST   A, (RD1)+
```

(a)MISO system-based

```
CLR  A
LD   #D0_ADR, RS0
ST   #N, BRC
BRPT end_block0
LD   RT0, A
MAC  (RS0), (RC0)+, A
ST   A, RT0
LD   RT2, A
MAC  (RS0)+, (RC2)+, A
ST   A, RT2
; end_block0
CLR  A
LD   #D1_ADR, RS1
ST   #N, BRC
BRPT end_block1
LD   RT1, A
MAC  (RS1), (RC1)+, A
ST   A, RT1
LD   RT3, A
MAC  (RS1)+, (RC3)+, A
ST   A, RT3
; end_block1
ADD  RT0, RT1, (RD0)+
ADD  RT2, RT3, (RD1)+
```

(b)SIMO system-based

Fig. 7 Procedure with a single MAC unit of one accumulator ($\texttt{MAC}^{(1)} \times 1$).

```
CLR  A
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC0)+, A
RPT  #N
MAC  (RS1)+, (RC1)+, A
ST   A, (RD0)+
CLR  B
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC2)+, B
RPT  #N
MAC  (RS1)+, (RC3)+, B
ST   B, (RD1)+
```

(a)MISO system-based

```
CLR  A
CLR  B
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #2(N+1)
MAC  (RS0){+}, (RC0)+/(RC2)+, A/B
RPT  #2(N+1)
MAC  (RS1){+}, (RC1)+/(RC3)+, A/B
ST   A, (RD0)+
ST   B, (RD1)+
```

(b)SIMO system-based

Fig. 8 Procedure with a single MAC unit of two accumulators ($\texttt{MAC}^{(2)} \times 1$).

Fig. 6.

- $\texttt{RC}_n$: The register containing the address of the polyphase filter coefficients. RC0, RC1, RC2 and RC3 are for $P_{0,0}(z)$, $P_{0,1}(z)$, $P_{1,0}(z)$ and $P_{1,1}(z)$ in Fig. 6, respectively.
- $\texttt{RD}_n$: The register containing the address of $W_n(z)$ in Fig. 6.
- $\texttt{RT}_n$: The n-th temporary register.
- BRC : Block repeat counter.

Figures 7, 8, 9 and 10 show the procedures for four different architectures in pseudo machine code. The code shown in Fig. 8(b) uses the MAC instruction with the multi-cycle increment function for the sake of simplification. To the author's knowledge, there is no DSP with this kind of function. On real processors, successive MAC instructions without and with increment will achieve this purpose at the expense of acceleration by the repeat instruction. On our assumptions, both of the approaches result in the same. Note that, in Fig. 10, two accumulators are sufficient and the code shown in Fig. 9 is directly applicable, although we use all of four accumulators A,B,C and D.

```
CLR  A
CLR  C
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC0)+, A || MAC (RS1)+, (RC1)+, C
ADD  A, C, (RD0)+
CLR  A
CLR  C
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC2)+, A || MAC (RS1)+, (RC3)+, C
ADD  A, C, (RD1)+
```

(a)MISO system-based

```
CLR  A
CLR  C
LD   #D0_ADR, RS0
ST   #N, BRC
BRPT end_block0
LD   RT0, A
LD   RT2, C
MAC  (RS0)+, (RC0)+, A || MAC (RS0)+, (RC2)+, C
ST   A, RT0
ST   C, RT2
; end_block0
CLR  A
CLR  C
LD   #D1_ADR, RS1
ST   #N, BRC
BRPT end_block1
LD   RT1, A
LD   RT3, C
MAC  (RS1), (RC1)+, A || MAC  (RS1)+, (RC3)+, C
ST   A, RT1
ST   C, RT3
; end_block1
ADD  RT0, RT1, (RD0)+
ADD  RT2, RT3, (RD1)+
```

(b)SIMO system-based

Fig. 9 Procedure with dual MAC units of one accumulator ($\texttt{MAC}^{(1)} \times 2$).

```
CLR  A
CLR  C
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC0)+, A || MAC (RS1)+, (RC1)+, C
ADD  A, C, (RD0)+
CLR  B
CLR  D
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC2)+, B || MAC (RS1)+, (RC3)+, D
ADD  B, D, (RD1)+
```

(a)MISO system-based

```
CLR  A
CLR  C
LD   #D0_ADR, RS0
LD   #D1_ADR, RS1
RPT  #N
MAC  (RS0)+, (RC0)+, A || MAC  (RS0)+, (RC2)+ C
RPT  #N
MAC  (RS1)+, (RC1)+, A || MAC  (RS1)+, (RC3)+,C
ST   A, (RD0)+
ST   C, (RD1)+
```

(b)SIMO system-based

Fig. 10 Procedure with dual MAC units of two accumulators ($\texttt{MAC}^{(2)} \times 2$).

Table 2 The number of memory accesses per sample for two-channel filter banks.

	MISO system-based procedure					SIMO system-based procedure				
	Input read N_{RD}	Filter Coef. read N_{RC}	Temp. write N_{WR}	Temp. read N_{RT}	Output write N_{WT}	Input read N_{RD}	Filter Coef. read N_{RC}	Temp. write N_{WR}	Temp. read N_{RT}	Output write N_{WT}
$\mathtt{MAC}^{(1)} \times 1$	$2(N+1)$	$2(N+1)$	0	0	1	$(N+1)$	$2(N+1)$	$2(N+1)$	$2(N+1)$	1
$\mathtt{MAC}^{(2)} \times 1$	$2(N+1)$	$2(N+1)$	0	0	1	$(N+1)$	$2(N+1)$	2	2	1
$\mathtt{MAC}^{(1)} \times 2$	$2(N+1)$	$2(N+1)$	0	0	1	$(N+1)$	$2(N+1)$	0	0	1
$\mathtt{MAC}^{(2)} \times 2$	$2(N+1)$	$2(N+1)$	0	0	1	$(N+1)$	$2(N+1)$	0	0	1

Table 3 Differences of the power consumption between MISO system-based and SIMO system-based procedures.

	The power of MISO system-based procedure minus the power SIMO system-based procedure
$\mathtt{MAC}^{(1)} \times 1$	$\frac{1}{2F_S}V^2\{(N+1)C'_{\mathrm{RD}} - M(N+1)(C'_{\mathrm{RT}} + C'_{\mathrm{WT}})\} + (P_{\mathrm{M1}} - P_{\mathrm{S1}})$
$\mathtt{MAC}^{(2)} \times 1$	$\frac{1}{2F_S}V^2\{(N+1)C'_{\mathrm{RD}} - M(C'_{\mathrm{RT}} + C'_{\mathrm{WT}})\} + (P_{\mathrm{M2}} - P_{\mathrm{S2}})$
$\mathtt{MAC}^{(1)} \times 2$	$\frac{1}{2F_S}V^2\{(N+1)C'_{\mathrm{RD}}\} + M(P_{\mathrm{M1}} - P_{\mathrm{S1}})$
$\mathtt{MAC}^{(2)} \times 2$	$\frac{1}{2F_S}V^2\{(N+1)C'_{\mathrm{RD}}\} + M(P_{\mathrm{M2}} - P_{\mathrm{S2}})$

4.2 The Number of Memory Access

On the assumption made in Sect. 3.1, we consider the number of memory accesses involved in the procedures shown in Sect. 4.1.

Table 2 shows the estimated number of memory accesses per sample, that is either of input or output sample, where we counted the numbers of MAC operation, ADD operation, load and store instructions from Figs. 7, 8, 9 and 10. The notation $\mathtt{MAC}^{(L)} \times K$ means DSP with K MAC units of L accumulators. In total, there are KL accumulators.

From Table 2, we see that:

- The number of input read of MISO system-based procedure is twice as large as that of SIMO system-based one. While the multi-cycle increment/decrement function is supported, this statement is true.
- The number of memory accesses does not depend on the number of MAC units and accumulators for MISO system-based procedure.
- The SIMO system-based procedure requires memory accesses for temporal data read and write, except for $\mathtt{MAC}^{(2)}$.

4.3 Power Consumption

For reference, let us consider the power consumption [6]. Since the switching power occupies most of the power consumption, we briefly show the estimation of that. Let P_{RD}, P_{RC}, P_{WR}, P_{RT} and P_{WT} denote the switching power of data read, filter-coefficient read, result write, temporary read and write, respectively, and let P_{MAC} be the switching power consumed in the MAC unit. Then, the switching power consumption P can be represented as follows:

$$P = P_{\mathrm{RD}} + P_{\mathrm{RC}} + P_{\mathrm{WR}} + P_{\mathrm{RT}} + P_{\mathrm{WT}} + P_{\mathrm{MAC}}. \tag{7}$$

When the word length is B, each term of the right hand side of Eq. (7) is given by $P_X = \sum_{i=0}^{B-1} \frac{1}{2} C_X V^2 TR_X(i)$, where X is one of memory access types, that is $X \in \{\mathrm{RD}, \mathrm{RC}, \mathrm{WR}, \mathrm{RT}, \mathrm{WT}\}$. C_{RD}, C_{RC}, C_{WR}, C_{WT} and C_{WT} are capacitances for the corresponding memory accesses, respectively. The amount of capacitance depends on the memory type, memory location, bus length, I/O pad and so forth [5], [6]. The notation $TR_X(i)$ denotes the i-th bit toggle rate of each access type. V is the supplied voltage.

The toggle rate $TR_X(i)$ can be represented as $TR_X(i) = \rho_X(i) N_X / F_S$, where $\rho_X(i)$ is the i-th bit alteration ratio for $0 \le \rho_X(i) \le 1$, N_X is the number of memory transfers per output, and the equality in Eq. (6) is assumed to hold. When $\rho_X(i)$ are independent from the access type and the bit number and equal to a constant value ρ, P can be reduced to

$$P = \frac{1}{2} V^2 \sum_{X \in \mathcal{S}} C'_X N_X + P_{\mathrm{MAC}}, \tag{8}$$

where we define the effective capacitance C'_X by $C'_X = \rho B C_X$ [6], and $\mathcal{S} = \{\mathrm{RD}, \mathrm{RC}, \mathrm{WR}, \mathrm{RT}, \mathrm{WT}\}$.

Table 3 shows the differences of the power consumption between MISO and SIMO system-based procedures, where the power consumption of SIMO system-based procedure is subtracted from that of MISO system-based one. P_{Mn} and P_{Sn} are the power consumption of MAC unit P_{MAC} with n accumulators for the MISO and SIMO system-based procedures, respectively. For the two-channel case, M equals 2.

Usually, C'_{RT} and C'_{WT} are capacitances of on-chip registers and smaller than the others. C'_{RD}, C'_{RC} and C'_{WR} are capacitances of either of on-chip or off-chip memories. When the input data are read from off-chip memory, C'_{RD} becomes larger than the on-chip case [6]. So does C'_{RC}. When the result is written out to off-chip

memory, the similar statement holds. P_{Mn} and P_{Sn} are comparable to each other.

From Table 2, we see that:

- For $\mathtt{MAC}^{(1)} \times 1$, when C'_{RD} is much larger than $M(C'_{\mathrm{RT}} + C'_{\mathrm{WT}})$, SIMO system-based procedure consumes less power than MISO system-based one.
- For $\mathtt{MAC}^{(1)} \times 2$, when C'_{RD} is much larger than $M(C'_{\mathrm{RT}} + C'_{\mathrm{WT}})/(N+1)$, SIMO system-based procedure consumes less power than MISO system-based one.
- For $\mathtt{MAC}^{(1)} \times 2$ and $\mathtt{MAC}^{(2)} \times 2$, if C'_{RD} gets much larger, the SIMO system-based procedure consumes less power than the MISO system-based one.
- For $\mathtt{MAC}^{(1)} \times 1$, $\mathtt{MAC}^{(1)} \times 2$ and $\mathtt{MAC}^{(2)} \times 2$, the deference of the power consumptions increase proportionally with the order of N.

4.4 Processing Accuracy

When data in accumulators are stored into a register or memory, rounding is applied to make the length fit to the destination. Usually, saturation process is also applied when either of overflow or underflow causes. These processes influence the processing accuracy. For $\mathtt{MAC}^{(1)} \times 1$, the SIMO system-based procedure requires redundant temporary accesses. However, with the MISO system-based one, these accesses do not cause. This fact implies that the processing accuracy is influenced by not only the architecture but also the procedure. Let us investigate the processing accuracy of the SIMO system-based procedure with the following condition:

- Data are integer. Filter coefficients are integer with a divisor of a power of 2.
- During accumulation, neither of rounding nor saturation is assumed to cause, since accumulators are assumed to have enough length.
- Rounding, saturation and right shift for division are assumed to be applied while transferring data from accumulator to memory.
- Input sequence is generated by a random process with the dynamic range varying from 1 to 32 bits as signed data.
- All operations in the ideal process to be compared are double precision.

Figures 11(a) and (b) show the processing accuracy of the SIMO system-based procedures with $\mathtt{MAC}^{(1)} \times 1$ and with $\mathtt{MAC}^{(2)} \times 1$, where Figs. 11(a) and (b) correspond to the word lengths of 16 bits and of 32 bits, respectively. In Fig. 11, the signal-to-noise ratio (SNR) is investigated for word lengths of 16 and 32 bits, respectively, where the biorthognal wavelet of 9/7 tap filters is used [9].

From Fig. 11, it is noticed that processing accuracy of $\mathtt{MAC}^{(2)} \times 1$ is better than that of $\mathtt{MAC}^{(1)} \times 1$.

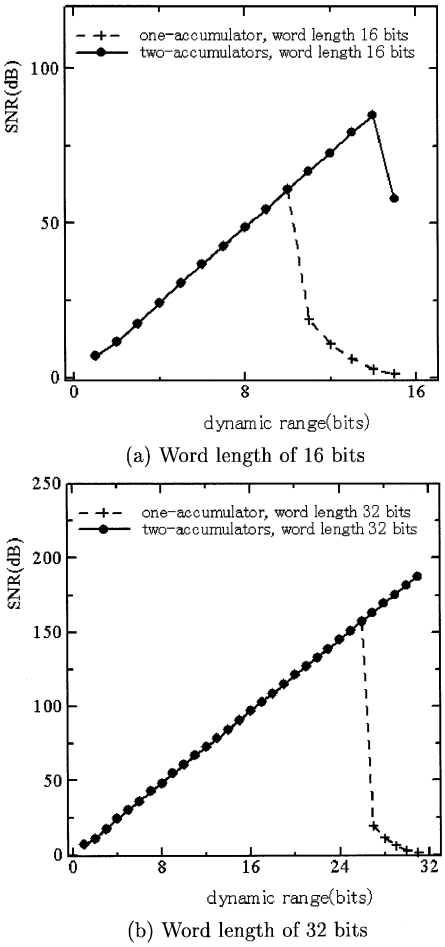

Fig. 11 Amplitude range vs. SNR for the SIMO system-based procedure, which shows the rounding and overflow/underflow effects.

For $\mathtt{MAC}^{(1)} \times 1$, there is a drop at smaller rage of input. This is because that the saturation causes more frequently due to the temporary write accesses. Note that MISO system-based procedure does not require temporary write accesses at all as well as the case of more than two accumulators. It is obvious that fewer saturation events happen. In summary, processing accuracy should be taken care of when selecting the SIMO system-based procedure.

4.5 Required Instruction Cycles

The number of memory accesses influences the required instruction cycles, that is the processing speed. So far it has been assumed that a single MAC operation completes in a single instruction cycle. It, however, depends on the type and location of the accessed memory due to wait cycles inserted for timing compensation. Thus, it is worth discussing the required instruction cycles.

In general, DRAM consumes more instruction cycles than SRAM. In addition, an off-chip memory consumes more instruction cycles than an on-chip memory.

Table 4 The number of memory accesses per sample for M-channel filter banks.

	MISO system-based procedure					SIMO system-based procedure				
	Input read N_{RD}	Filter Coef. read N_{RC}	Temp. write N_{WR}	Temp. read N_{RT}	Output write N_{WT}	Input read N_{RD}	Filter Coef. read N_{RC}	Temp. write N_{WR}	Temp. read N_{RT}	Output write N_{WT}
$\mathtt{MAC}^{(1)} \times 1$	$M(N+1)$	$M(N+1)$	0	0	1	$N+1$	$M(N+1)$	$M(N+1)$	$M(N+1)$	1
$\mathtt{MAC}^{(M)} \times 1$	$M(N+1)$	$M(N+1)$	0	0	1	$N+1$	$M(N+1)$	M	M	1
$\mathtt{MAC}^{(1)} \times M$	$M(N+1)$	$M(N+1)$	0	0	1	$N+1$	$M(N+1)$	0	0	1
$\mathtt{MAC}^{(M)} \times M$	$M(N+1)$	$M(N+1)$	0	0	1	$N+1$	$M(N+1)$	0	0	1

From these facts, the memory accesses to read or write data are likely to require a lot of instruction cycles because an off-chip DRAM is frequently used for storing data. In this sense, the procedure which requires less memory access for data input and output is desirable to implement filter banks.

Let w be the number of wait cycles inserted for accessing off-chip memories. Then, from Figs. 7, 8, 9 and 10, the condition in Eq. (6) can be rewritten as follows:

$$F_{\mathrm{clk}} \geq [\{M(N+1)-1\}/K + w(2N+3)]F_S \quad (9)$$

for the MISO system-based procedure on $\mathtt{MAC}^{(1)} \times 1$ and $\mathtt{MAC}^{(2)} \times 1$, and

$$F_{\mathrm{clk}} \geq [\{M(N+1)-1\}/K + w(N+2)]F_S \quad (10)$$

for the SIMO system-based procedure on $\mathtt{MAC}^{(1)} \times 1$ and $\mathtt{MAC}^{(2)} \times 1$. In the case of dual MAC units, the condition is given by Eq. (10) for both procedures. As a result, we see that the SIMO system-based procedure is preferable in terms of the processing speed as well as the power consumption.

5. M-Channel Case

We discussed the memory access estimation of two-channel filter banks. In this section, we consider extending the discussion to the M-channel case.

From the similar way to Sect. 4, the number of memory accesses for M-channel filter banks is obtained as shown in Table 4, where $\mathtt{MAC}^{(\mathtt{M})} \times \mathtt{1}$ and $\mathtt{MAC}^{(\mathtt{M})} \times \mathtt{M}$ use M accumulators as shown in Fig. 5.

If the number of channels is large, the SIMO system-based procedure influences the number of memory accesses. Because the number of input data accesses is one M-th of that for MISO system-based one. Therefore, we can obtain the following results:

For MISO system-based procedure, $\mathtt{MAC}^{(1)} \times \mathtt{M}$ and $\mathtt{MAC}^{(\mathtt{M})} \times \mathtt{M}$ require the least number of memory accesses. Therefore, $\mathtt{MAC}^{(1)} \times \mathtt{M}$ is the most effective in terms of the number of memory accesses. Also the power consumption can be led as shown in Table 3 in the same way to the discussion in Sect. 4.3. Actually, M accumulators are in total enough to implement M-channel filter banks.

6. Conclusions

In this paper, the DSP implementation of filter banks was investigated for different architectures by introducing a unified polyphase representation of analysis and synthesis banks. Especially, the number of memory accesses was discussed. The power consumptions, the processing accuracies and the required instruction cycles were also dealt with. It was shown that the number of data read in SIMO system-based procedure was a half of that in MISO system-based one for two-channel filter banks. This fact implies that SIMO system-based procedure is preferable in terms of the power consumption and the processing speed. However, for the processing accuracy, it was shown that the SIMO system-based procedure should be taken care of when the MAC unit is single.

In future, we will consider investigating of the lifting scheme. The lifting scheme is regarded as a cascade of sparse polyphase matrices [2], [7]. Thus, some parts of this work are applicable. We are also interested in developing a DSP with multi-cycle increment functionality for the combination of the MAC and repeat instructions.

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